<?xml version="1.0" encoding="UTF-8" standalone="no"?>

<board schema\_version="2.0" vendor="allaboutfpga.com" name="edgeA7" display\_name="edgeA7" url="https://allaboutfpga.com" preset\_file="preset.xml">

<images>

<image name="edge\_artix7.jpg" display\_name="EDGE Artix 7 BOARD" sub\_type="board">

<description>EDGE Artix 7 Board File Image</description>

</image>

</images>

<compatible\_board\_revisions>

<revision id="0">1.0</revision>

</compatible\_board\_revisions>

<file\_version>1.1</file\_version>

<description>edgeA7</description>

<components>

<component name="part0" display\_name="edgeA7" type="fpga" part\_name="xc7a35tftg256-1" pin\_map\_file="part0\_pins.xml" vendor="xilinx" spec\_url="https://allaboutfpga.com">

<interfaces>

<interface mode="master" name="cellular\_ram" type="xilinx.com:interface:emc\_rtl:1.0" of\_component="cellular\_ram" preset\_proc="sram\_preset">

<description>512KB SRAM</description>

<port\_maps>

<port\_map logical\_port="ADDR" physical\_port="cellular\_ram\_addr" dir="inout" left="18" right="0">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="cellular\_ram\_addr\_0"/>

<pin\_map port\_index="1" component\_pin="cellular\_ram\_addr\_1"/>

<pin\_map port\_index="2" component\_pin="cellular\_ram\_addr\_2"/>

<pin\_map port\_index="3" component\_pin="cellular\_ram\_addr\_3"/>

<pin\_map port\_index="4" component\_pin="cellular\_ram\_addr\_4"/>

<pin\_map port\_index="5" component\_pin="cellular\_ram\_addr\_5"/>

<pin\_map port\_index="6" component\_pin="cellular\_ram\_addr\_6"/>

<pin\_map port\_index="7" component\_pin="cellular\_ram\_addr\_7"/>

<pin\_map port\_index="8" component\_pin="cellular\_ram\_addr\_8"/>

<pin\_map port\_index="9" component\_pin="cellular\_ram\_addr\_9"/>

<pin\_map port\_index="10" component\_pin="cellular\_ram\_addr\_10"/>

<pin\_map port\_index="11" component\_pin="cellular\_ram\_addr\_11"/>

<pin\_map port\_index="12" component\_pin="cellular\_ram\_addr\_12"/>

<pin\_map port\_index="13" component\_pin="cellular\_ram\_addr\_13"/>

<pin\_map port\_index="14" component\_pin="cellular\_ram\_addr\_14"/>

<pin\_map port\_index="15" component\_pin="cellular\_ram\_addr\_15"/>

<pin\_map port\_index="16" component\_pin="cellular\_ram\_addr\_16"/>

<pin\_map port\_index="17" component\_pin="cellular\_ram\_addr\_17"/>

<pin\_map port\_index="18" component\_pin="cellular\_ram\_addr\_18"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="DQ\_O" physical\_port="cellular\_ram\_dq\_o" dir="out" left="7" right="0">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="cellular\_ram\_dq\_0"/>

<pin\_map port\_index="1" component\_pin="cellular\_ram\_dq\_1"/>

<pin\_map port\_index="2" component\_pin="cellular\_ram\_dq\_2"/>

<pin\_map port\_index="3" component\_pin="cellular\_ram\_dq\_3"/>

<pin\_map port\_index="4" component\_pin="cellular\_ram\_dq\_4"/>

<pin\_map port\_index="5" component\_pin="cellular\_ram\_dq\_5"/>

<pin\_map port\_index="6" component\_pin="cellular\_ram\_dq\_6"/>

<pin\_map port\_index="7" component\_pin="cellular\_ram\_dq\_7"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="DQ\_I" physical\_port="cellular\_ram\_dq\_i" dir="in" left="7" right="0">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="cellular\_ram\_dq\_0"/>

<pin\_map port\_index="1" component\_pin="cellular\_ram\_dq\_1"/>

<pin\_map port\_index="2" component\_pin="cellular\_ram\_dq\_2"/>

<pin\_map port\_index="3" component\_pin="cellular\_ram\_dq\_3"/>

<pin\_map port\_index="4" component\_pin="cellular\_ram\_dq\_4"/>

<pin\_map port\_index="5" component\_pin="cellular\_ram\_dq\_5"/>

<pin\_map port\_index="6" component\_pin="cellular\_ram\_dq\_6"/>

<pin\_map port\_index="7" component\_pin="cellular\_ram\_dq\_7"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="DQ\_T" physical\_port="cellular\_ram\_dq\_t" dir="out" left="7" right="0">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="cellular\_ram\_dq\_0"/>

<pin\_map port\_index="1" component\_pin="cellular\_ram\_dq\_1"/>

<pin\_map port\_index="2" component\_pin="cellular\_ram\_dq\_2"/>

<pin\_map port\_index="3" component\_pin="cellular\_ram\_dq\_3"/>

<pin\_map port\_index="4" component\_pin="cellular\_ram\_dq\_4"/>

<pin\_map port\_index="5" component\_pin="cellular\_ram\_dq\_5"/>

<pin\_map port\_index="6" component\_pin="cellular\_ram\_dq\_6"/>

<pin\_map port\_index="7" component\_pin="cellular\_ram\_dq\_7"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="OEN" physical\_port="cellular\_ram\_oen" dir="inout">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="cellular\_ram\_oen"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="WEN" physical\_port="cellular\_ram\_wen" dir="inout">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="cellular\_ram\_wen"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="CE\_N" physical\_port="cellular\_ram\_ce\_n" dir="inout">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="cellular\_ram\_ce\_n"/>

</pin\_maps>

</port\_map>

</port\_maps>

</interface>

<interface mode="master" name="dip\_switches\_16bits" type="xilinx.com:interface:gpio\_rtl:1.0" of\_component="dip\_switches\_16bits" preset\_proc="dip\_switches\_16bits\_preset">

<port\_maps>

<port\_map logical\_port="TRI\_I" physical\_port="dip\_switches\_16bits\_tri\_i" dir="in" left="15" right="0">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="dip\_switches\_16bits\_tri\_i\_0"/>

<pin\_map port\_index="1" component\_pin="dip\_switches\_16bits\_tri\_i\_1"/>

<pin\_map port\_index="2" component\_pin="dip\_switches\_16bits\_tri\_i\_2"/>

<pin\_map port\_index="3" component\_pin="dip\_switches\_16bits\_tri\_i\_3"/>

<pin\_map port\_index="4" component\_pin="dip\_switches\_16bits\_tri\_i\_4"/>

<pin\_map port\_index="5" component\_pin="dip\_switches\_16bits\_tri\_i\_5"/>

<pin\_map port\_index="6" component\_pin="dip\_switches\_16bits\_tri\_i\_6"/>

<pin\_map port\_index="7" component\_pin="dip\_switches\_16bits\_tri\_i\_7"/>

<pin\_map port\_index="8" component\_pin="dip\_switches\_16bits\_tri\_i\_8"/>

<pin\_map port\_index="9" component\_pin="dip\_switches\_16bits\_tri\_i\_9"/>

<pin\_map port\_index="10" component\_pin="dip\_switches\_16bits\_tri\_i\_10"/>

<pin\_map port\_index="11" component\_pin="dip\_switches\_16bits\_tri\_i\_11"/>

<pin\_map port\_index="12" component\_pin="dip\_switches\_16bits\_tri\_i\_12"/>

<pin\_map port\_index="13" component\_pin="dip\_switches\_16bits\_tri\_i\_13"/>

<pin\_map port\_index="14" component\_pin="dip\_switches\_16bits\_tri\_i\_14"/>

<pin\_map port\_index="15" component\_pin="dip\_switches\_16bits\_tri\_i\_15"/>

</pin\_maps>

</port\_map>

</port\_maps>

</interface>

<interface mode="master" name="led\_16bits" type="xilinx.com:interface:gpio\_rtl:1.0" of\_component="led\_16bits" preset\_proc="led\_16bits\_preset">

<port\_maps>

<port\_map logical\_port="TRI\_O" physical\_port="led\_16bits\_tri\_o" dir="out" left="15" right="0">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="led\_16bits\_tri\_o\_0"/>

<pin\_map port\_index="1" component\_pin="led\_16bits\_tri\_o\_1"/>

<pin\_map port\_index="2" component\_pin="led\_16bits\_tri\_o\_2"/>

<pin\_map port\_index="3" component\_pin="led\_16bits\_tri\_o\_3"/>

<pin\_map port\_index="4" component\_pin="led\_16bits\_tri\_o\_4"/>

<pin\_map port\_index="5" component\_pin="led\_16bits\_tri\_o\_5"/>

<pin\_map port\_index="6" component\_pin="led\_16bits\_tri\_o\_6"/>

<pin\_map port\_index="7" component\_pin="led\_16bits\_tri\_o\_7"/>

<pin\_map port\_index="8" component\_pin="led\_16bits\_tri\_o\_8"/>

<pin\_map port\_index="9" component\_pin="led\_16bits\_tri\_o\_9"/>

<pin\_map port\_index="10" component\_pin="led\_16bits\_tri\_o\_10"/>

<pin\_map port\_index="11" component\_pin="led\_16bits\_tri\_o\_11"/>

<pin\_map port\_index="12" component\_pin="led\_16bits\_tri\_o\_12"/>

<pin\_map port\_index="13" component\_pin="led\_16bits\_tri\_o\_13"/>

<pin\_map port\_index="14" component\_pin="led\_16bits\_tri\_o\_14"/>

<pin\_map port\_index="15" component\_pin="led\_16bits\_tri\_o\_15"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="TRI\_I" physical\_port="led\_16bits\_tri\_o" dir="in" left="15" right="0">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="led\_16bits\_tri\_o\_0"/>

<pin\_map port\_index="1" component\_pin="led\_16bits\_tri\_o\_1"/>

<pin\_map port\_index="2" component\_pin="led\_16bits\_tri\_o\_2"/>

<pin\_map port\_index="3" component\_pin="led\_16bits\_tri\_o\_3"/>

<pin\_map port\_index="4" component\_pin="led\_16bits\_tri\_o\_4"/>

<pin\_map port\_index="5" component\_pin="led\_16bits\_tri\_o\_5"/>

<pin\_map port\_index="6" component\_pin="led\_16bits\_tri\_o\_6"/>

<pin\_map port\_index="7" component\_pin="led\_16bits\_tri\_o\_7"/>

<pin\_map port\_index="8" component\_pin="led\_16bits\_tri\_o\_8"/>

<pin\_map port\_index="9" component\_pin="led\_16bits\_tri\_o\_9"/>

<pin\_map port\_index="10" component\_pin="led\_16bits\_tri\_o\_10"/>

<pin\_map port\_index="11" component\_pin="led\_16bits\_tri\_o\_11"/>

<pin\_map port\_index="12" component\_pin="led\_16bits\_tri\_o\_12"/>

<pin\_map port\_index="13" component\_pin="led\_16bits\_tri\_o\_13"/>

<pin\_map port\_index="14" component\_pin="led\_16bits\_tri\_o\_14"/>

<pin\_map port\_index="15" component\_pin="led\_16bits\_tri\_o\_15"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="TRI\_T" physical\_port="led\_16bits\_tri\_o" dir="out" left="15" right="0">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="led\_16bits\_tri\_o\_0"/>

<pin\_map port\_index="1" component\_pin="led\_16bits\_tri\_o\_1"/>

<pin\_map port\_index="2" component\_pin="led\_16bits\_tri\_o\_2"/>

<pin\_map port\_index="3" component\_pin="led\_16bits\_tri\_o\_3"/>

<pin\_map port\_index="4" component\_pin="led\_16bits\_tri\_o\_4"/>

<pin\_map port\_index="5" component\_pin="led\_16bits\_tri\_o\_5"/>

<pin\_map port\_index="6" component\_pin="led\_16bits\_tri\_o\_6"/>

<pin\_map port\_index="7" component\_pin="led\_16bits\_tri\_o\_7"/>

<pin\_map port\_index="8" component\_pin="led\_16bits\_tri\_o\_8"/>

<pin\_map port\_index="9" component\_pin="led\_16bits\_tri\_o\_9"/>

<pin\_map port\_index="10" component\_pin="led\_16bits\_tri\_o\_10"/>

<pin\_map port\_index="11" component\_pin="led\_16bits\_tri\_o\_11"/>

<pin\_map port\_index="12" component\_pin="led\_16bits\_tri\_o\_12"/>

<pin\_map port\_index="13" component\_pin="led\_16bits\_tri\_o\_13"/>

<pin\_map port\_index="14" component\_pin="led\_16bits\_tri\_o\_14"/>

<pin\_map port\_index="15" component\_pin="led\_16bits\_tri\_o\_15"/>

</pin\_maps>

</port\_map>

</port\_maps>

</interface>

<interface mode="master" name="push\_buttons\_4bits" type="xilinx.com:interface:gpio\_rtl:1.0" of\_component="push\_buttons\_4bits" preset\_proc="push\_buttons\_4bits\_preset">

<port\_maps>

<port\_map logical\_port="TRI\_I" physical\_port="push\_buttons\_4bits\_tri\_i" dir="in" left="3" right="0">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="push\_buttons\_5bits\_tri\_i\_0"/>

<pin\_map port\_index="1" component\_pin="push\_buttons\_5bits\_tri\_i\_1"/>

<pin\_map port\_index="2" component\_pin="push\_buttons\_5bits\_tri\_i\_2"/>

<pin\_map port\_index="3" component\_pin="push\_buttons\_5bits\_tri\_i\_3"/>

</pin\_maps>

</port\_map>

</port\_maps>

</interface>

<interface mode="master" name="qspi\_flash" type="xilinx.com:interface:spi\_rtl:1.0" of\_component="qspi\_flash" preset\_proc="qspi\_preset">

<description>Quad SPI Flash</description>

<preferred\_ips>

<preferred\_ip vendor="xilinx.com" library="ip" name="axi\_quad\_spi" order="0"/>

</preferred\_ips>

<port\_maps>

<port\_map logical\_port="IO0\_I" physical\_port="qspi\_db0\_i" dir="in">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_db0\_i"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="IO0\_O" physical\_port="qspi\_db0\_o" dir="out">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_db0\_i"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="IO0\_T" physical\_port="qspi\_db0\_t" dir="out">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_db0\_i"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="IO1\_I" physical\_port="qspi\_db1\_i" dir="in">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_db1\_i"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="IO1\_O" physical\_port="qspi\_db1\_o" dir="out">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_db1\_i"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="IO1\_T" physical\_port="qspi\_db1\_t" dir="out">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_db1\_i"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="IO2\_I" physical\_port="qspi\_db2\_i" dir="in">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_db2\_i"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="IO2\_O" physical\_port="qspi\_db2\_o" dir="out">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_db2\_i"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="IO2\_T" physical\_port="qspi\_db2\_t" dir="out">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_db2\_i"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="IO3\_I" physical\_port="qspi\_db3\_i" dir="in">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_db3\_i"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="IO3\_O" physical\_port="qspi\_db3\_o" dir="out">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_db3\_i"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="IO3\_T" physical\_port="qspi\_db3\_t" dir="out">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_db3\_i"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="SS\_I" physical\_port="qspi\_csn\_i" dir="in">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_csn\_i"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="SS\_O" physical\_port="qspi\_csn\_o" dir="out">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_csn\_i"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="SS\_T" physical\_port="qspi\_csn\_t" dir="out">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="qspi\_csn\_i"/>

</pin\_maps>

</port\_map>

</port\_maps>

</interface>

<interface mode="slave" name="reset" type="xilinx.com:signal:reset\_rtl:1.0" of\_component="reset">

<port\_maps>

<port\_map logical\_port="RST" physical\_port="reset" dir="in">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="reset"/>

</pin\_maps>

</port\_map>

</port\_maps>

<parameters>

<parameter name="rst\_polarity" value="1" />

</parameters>

</interface>

<interface mode="master" name="seven\_seg\_led\_an" type="xilinx.com:interface:gpio\_rtl:1.0" of\_component="seven\_seg\_led\_an" preset\_proc="seven\_seg\_led\_an\_preset">

<port\_maps>

<port\_map logical\_port="TRI\_O" physical\_port="seven\_seg\_led\_an\_tri\_o" dir="out" left="3" right="0">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="seven\_seg\_led\_an\_tri\_o\_0"/>

<pin\_map port\_index="1" component\_pin="seven\_seg\_led\_an\_tri\_o\_1"/>

<pin\_map port\_index="2" component\_pin="seven\_seg\_led\_an\_tri\_o\_2"/>

<pin\_map port\_index="3" component\_pin="seven\_seg\_led\_an\_tri\_o\_3"/>

</pin\_maps>

</port\_map>

</port\_maps>

</interface>

<interface mode="master" name="seven\_seg\_led\_disp" type="xilinx.com:interface:gpio\_rtl:1.0" of\_component="seven\_seg\_led\_disp" preset\_proc="seven\_seg\_led\_seg\_preset">

<port\_maps>

<port\_map logical\_port="TRI\_O" physical\_port="seven\_seg\_led\_disp\_tri\_o" dir="out" left="7" right="0">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="seven\_seg\_led\_disp\_tri\_o\_0"/>

<pin\_map port\_index="1" component\_pin="seven\_seg\_led\_disp\_tri\_o\_1"/>

<pin\_map port\_index="2" component\_pin="seven\_seg\_led\_disp\_tri\_o\_2"/>

<pin\_map port\_index="3" component\_pin="seven\_seg\_led\_disp\_tri\_o\_3"/>

<pin\_map port\_index="4" component\_pin="seven\_seg\_led\_disp\_tri\_o\_4"/>

<pin\_map port\_index="5" component\_pin="seven\_seg\_led\_disp\_tri\_o\_5"/>

<pin\_map port\_index="6" component\_pin="seven\_seg\_led\_disp\_tri\_o\_6"/>

<pin\_map port\_index="7" component\_pin="seven\_seg\_led\_disp\_tri\_o\_7"/>

</pin\_maps>

</port\_map>

</port\_maps>

</interface>

<interface mode="slave" name="sys\_clock" type="xilinx.com:signal:clock\_rtl:1.0" of\_component="sys\_clock" preset\_proc="sys\_clock\_preset">

<port\_maps>

<port\_map logical\_port="CLK" physical\_port="clk" dir="in">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="clk"/>

</pin\_maps>

</port\_map>

</port\_maps>

<parameters>

<parameter name="frequency" value="50000000" />

</parameters>

</interface>

<interface mode="master" name="usb\_uart" type="xilinx.com:interface:uart\_rtl:1.0" of\_component="usb\_uart" preset\_proc="uart\_preset">

<port\_maps>

<port\_map logical\_port="TxD" physical\_port="usb\_uart\_txd" dir="out">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="usb\_uart\_txd"/>

</pin\_maps>

</port\_map>

<port\_map logical\_port="RxD" physical\_port="usb\_uart\_rxd" dir="in">

<pin\_maps>

<pin\_map port\_index="0" component\_pin="usb\_uart\_rxd"/>

</pin\_maps>

</port\_map>

</port\_maps>

</interface>

</interfaces>

</component>

<component name="cellular\_ram" display\_name="Cell RAM" type="chip" sub\_type="memory\_flash\_bpi" major\_group="External Memory">

<description>512KB SRAM</description>

</component>

<component name="dip\_switches\_16bits" display\_name="16 Switches" type="chip" sub\_type="switch" major\_group="GPIO">

<description>Switches 15 to 0</description>

</component>

<component name="led\_16bits" display\_name="16 LEDs" type="chip" sub\_type="led" major\_group="GPIO">

<description>LEDs 15 to 0</description>

</component>

<component name="push\_buttons\_4bits" display\_name="4 Push Buttons" type="chip" sub\_type="push\_button" major\_group="GPIO">

<description>Push buttons 3 to 0 [Down Right Left Up]</description>

</component>

<component name="qspi\_flash" display\_name="QSPI Flash" type="chip" sub\_type="memory\_flash\_qspi" major\_group="External Memory">

<description>QSPI Flash</description>

</component>

<component name="reset" display\_name="Reset Signal (BTNC)" type="chip" sub\_type="reset" major\_group="Reset">

<description>Reset button (BTNC)</description>

</component>

<component name="seven\_seg\_led\_an" display\_name="7 Segment Display - Anodes" type="chip" sub\_type="led" major\_group="GPIO">

<description>Seven Segment Anodes</description>

</component>

<component name="seven\_seg\_led\_disp" display\_name="7 Segment Display - Segments" type="chip" sub\_type="led" major\_group="GPIO">

<description>Seven Segment display segments</description>

</component>

<component name="sys\_clock" display\_name="System Clock" type="chip" sub\_type="system\_clock" major\_group="Clocks">

<description>100 MHz System Clock</description>

</component>

<component name="usb\_uart" display\_name="USB UART" type="chip" sub\_type="uart" major\_group="UART">

<description>USB UART</description>

</component>

</components>

<jtag\_chains>

<jtag\_chain name="chain1">

<position name="0" component="part0"/>

</jtag\_chain>

</jtag\_chains>

<connections>

<connection name="part0\_cellular\_ram" component1="part0" component2="cellular\_ram">

<connection\_map name="part0\_cellular\_ram\_1" c1\_st\_index="1" c1\_end\_index="30" c2\_st\_index="0" c2\_end\_index="29"/>

</connection>

<connection name="part0\_dip\_switches\_16bits" component1="part0" component2="dip\_switches\_16bits">

<connection\_map name="part0\_dip\_switches\_16bits\_1" c1\_st\_index="31" c1\_end\_index="46" c2\_st\_index="0" c2\_end\_index="15"/>

</connection>

<connection name="part0\_led\_16bits" component1="part0" component2="led\_16bits">

<connection\_map name="part0\_led\_16bits\_1" c1\_st\_index="47" c1\_end\_index="62" c2\_st\_index="0" c2\_end\_index="15"/>

</connection>

<connection name="part0\_push\_buttons\_5bits" component1="part0" component2="push\_buttons\_5bits">

<connection\_map name="part0\_push\_buttons\_5bits\_1" c1\_st\_index="63" c1\_end\_index="66" c2\_st\_index="0" c2\_end\_index="3"/>

</connection>

<connection name="part0\_qspi\_flash" component1="part0" component2="qspi\_flash">

<connection\_map name="part0\_qspi\_flash\_1" c1\_st\_index="67" c1\_end\_index="71" c2\_st\_index="0" c2\_end\_index="4"/>

</connection>

<connection name="part0\_reset" component1="part0" component2="reset">

<connection\_map name="part0\_reset\_1" c1\_st\_index="72" c1\_end\_index="72" c2\_st\_index="0" c2\_end\_index="0"/>

</connection>

<connection name="part0\_seven\_seg\_led\_an" component1="part0" component2="seven\_seg\_led\_an">

<connection\_map name="part0\_seven\_seg\_led\_an\_1" c1\_st\_index="73" c1\_end\_index="76" c2\_st\_index="0" c2\_end\_index="3"/>

</connection>

<connection name="part0\_seven\_seg\_led\_disp" component1="part0" component2="seven\_seg\_led\_disp">

<connection\_map name="part0\_seven\_seg\_led\_disp\_1" c1\_st\_index="77" c1\_end\_index="84" c2\_st\_index="0" c2\_end\_index="7"/>

</connection>

<connection name="part0\_sys\_clock" component1="part0" component2="sys\_clock">

<connection\_map name="part0\_sys\_clock\_1" c1\_st\_index="0" c1\_end\_index="0" c2\_st\_index="0" c2\_end\_index="0"/>

</connection>

<connection name="part0\_usb\_uart" component1="part0" component2="usb\_uart">

<connection\_map name="part0\_usb\_uart\_1" c1\_st\_index="85" c1\_end\_index="86" c2\_st\_index="0" c2\_end\_index="1"/>

</connection>

</connections>

</board>